AMENDMENTS TO THE CLAIMS

1. (currently amended) A variable gain amplifier, comprising:

an amplifying transistor which amplifies an input signal; and

a current path control section which adjusts a percentage ~~controls a size~~ of the amplifying transistor that contributes to amplification of the input signal and a path of a current through the amplifying transistor.

2. (original) The variable gain amplifier as set forth in claim 1, wherein:

the current path control section includes a current control transistor which controls a current flow through the amplifying transistor, said variable gain amplifier comprising: a plurality of unit circuits which are disposed parallel to one another, each having the amplifying transistor and the current control transistor, said unit circuits being connected to one another through signal inputs and signal outputs of the unit circuits.

3. (withdrawn) The variable gain amplifier as set forth in claim 2, wherein the amplifying transistor comprises an amplifying transistor differential pair.

4. (withdrawn) The variable gain amplifier as set forth in claim 3, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180° out of phase from each other.

5. (withdrawn) The variable gain amplifier as set forth in claim 3, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

6. (withdrawn) The variable gain amplifier as set forth in claim 2, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

7. (withdrawn) The variable gain amplifier as set forth in claim 2, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

8. (withdrawn) The variable gain amplifier as set forth in claim 2, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

9. (withdrawn) The variable gain amplifier as set forth in claim 2, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

10. (original) The variable gain amplifier as set forth in claim 2, wherein each unit circuit includes a switch control circuit which switches levels of operation control voltages for the current control transistor.

11. (withdrawn) The variable gain amplifier as set forth in claim 10, wherein the amplifying transistor makes up an amplifying transistor differential pair.

12. (withdrawn) The variable gain amplifier as set forth in claim 11, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180° out of phase from each other.

13. (withdrawn) The variable gain amplifier as set forth in claim 11, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and

differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

14. (withdrawn) The variable gain amplifier as set forth in claim 10, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

15. (withdrawn) The variable gain amplifier as set forth in claim 10, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

16. (withdrawn) The variable gain amplifier as set forth in claim 10, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs

and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

17. (withdrawn) The variable gain amplifier as set forth in claim 10, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

18. (original) The variable gain amplifier as set forth in claim 10, wherein common operation control voltages are inputted to the switch control circuit of each unit circuit.

19. (withdrawn) The variable gain amplifier as set forth in claim 18, wherein the amplifying transistor comprises an amplifying transistor differential pair.

20. (withdrawn) The variable gain amplifier as set forth in claim 19, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180ø out of phase from each other.

21. (withdrawn) The variable gain amplifier as set forth in claim 19, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

22. (withdrawn) The variable gain amplifier as set forth in claim 18, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

23. (withdrawn) The variable gain amplifier as set forth in claim 18, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

24. (withdrawn) The variable gain amplifier as set forth in claim 18, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

25. (withdrawn) The variable gain amplifier as set forth in claim 18, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

26. (withdrawn) The variable gain amplifier as set forth in claim 18, comprising:

a voltage generator which generates the operation control voltages for each unit circuit based on a switch control signal which switches outputs of the switch control circuit.

27. (withdrawn) The variable gain amplifier as set forth in claim 26, wherein the amplifying transistor comprises an amplifying transistor differential pair.

28. (withdrawn) The variable gain amplifier as set forth in claim 27, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180° out of phase from each other.

29. (withdrawn) The variable gain amplifier as set forth in claim 27, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

30. (withdrawn) The variable gain amplifier as set forth in claim 26, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

31. (withdrawn) The variable gain amplifier as set forth in claim 26, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

32. (withdrawn) The variable gain amplifier as set forth in claim 26, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

33. (withdrawn) The variable gain amplifier as set forth in claim 26, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

34. (withdrawn) The variable gain amplifier as set forth in claim 26, wherein:

the switch control signal takes a value of either 0 or 1 to activate or deactivate the current control transistor, and

a channel width of the amplifying transistor satisfies

$wi = W0 \times R^{i} - W0 \times R^{(i-1)}$,

where R is a constant which satisfies

$R = (Wk/W0)^{1/k}$,

where wi is a channel width of the amplifying transistor of the unit circuit which corresponds to the switch control signal of an ordinal number i (0, 1, 2, ..., k; where k is an integer of not less than 0), and Wi is a channel width of i numbers of amplifying transistors whose gain is obtained when i is increased step-wise from 0 by the increment of 1 to increase the number of activated unit circuits according to the operation control voltage which was selected according to the switch control signal to activate the unit circuits.

35. (withdrawn) The variable gain amplifier as set forth in claim 18, wherein the operation control voltages are voltages of two levels: one cutting a current flow into the unit circuits; and the other allowing a current flow into the unit circuits.

36. (withdrawn) The variable gain amplifier as set forth in claim 35, wherein the amplifying transistor comprises an amplifying transistor differential pair.

37. (withdrawn) The variable gain amplifier as set forth in claim 36, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and

the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180° out of phase from each other.

38. (withdrawn) The variable gain amplifier as set forth in claim 36, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair

and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

39. (withdrawn) The variable gain amplifier as set forth in claim 35, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

40. (withdrawn) The variable gain amplifier as set forth in claim 35, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

41. (withdrawn) The variable gain amplifier as set forth in claim 35, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

42. (withdrawn) The variable gain amplifier as set forth in claim 35, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

43. (withdrawn) The variable gain amplifier as set forth in claim 35, wherein the voltage generator varies the level of one of the operation control voltages according to

the number of unit circuits with no current supply, so as to control a total amount of a current flow through the remaining unit circuits.

44. (withdrawn) The variable gain amplifier as set forth in claim 43, wherein the voltage generator generates the operation control voltages so as to control and maintain the total amount of a current flow at a constant level.

45. (currently amended) The variable gain amplifier as set forth in claim 1, wherein the current path control section varies ~~a size~~ the percentage of the amplifying transistor, and controls and maintains a current flow through the amplifying transistor at a constant level.

46. (withdrawn) The variable gain amplifier as set forth in claim 45, wherein:

the current path control section includes a current control transistor which controls a current flow through the amplifying transistor,

said variable gain amplifier comprising:

a plurality of unit circuits which are disposed parallel to one another and connected to one another through signal inputs and signal outputs of the unit circuits, each of the unit circuits including the amplifying transistor, the current control transistor, an auxiliary current control transistor which makes up a current mirror with

the current control transistor, and a switch control circuit which switches levels of operation control voltages for the current control transistor and the auxiliary current control transistor; and

a current source which supplies a constant current to the auxiliary current control transistor.

47. (withdrawn) The variable gain amplifier as set forth in claim 46, wherein the amplifying transistor comprises an amplifying transistor differential pair.

48. (withdrawn) The variable gain amplifier as set forth in claim 47, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first and second transistor differential pairs to a power source,

wherein gates of transistors which make up the first transistor differential pair and the second transistor differential pair receive oscillation signals which are 180° out of phase from each other.

49. (withdrawn) The variable gain amplifier as set forth in claim 47, further comprising:

a first transistor differential pair and a second transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the first transistor differential pair and the second transistor differential pair, the first transistor differential pair and the second transistor differential pair being connected to a source via different sides of the differential outputs;

a third transistor differential pair and a fourth transistor differential pair, each being provided as the amplifying transistor differential pair, with differential outputs which are cross-connected to each other between the third transistor differential pair and the fourth transistor differential pair, the third transistor differential pair and the fourth transistor differential pair being connected to a source via different sides of the differential outputs; and

a load impedance which connects outputs of the first through fourth transistor differential pairs to a power source,

wherein differential inputs of the first and second transistor differential pairs receive first oscillation signals which are 180° out of phase from each other, and differential inputs of the third and fourth transistor differential pairs receive a second oscillation signal which is 90° out of phase from the first oscillation signals.

50. (withdrawn) The variable gain amplifier as set forth in claim 46, wherein respective outputs of the unit circuits are connected to a power source via a load impedance.

51. (withdrawn) The variable gain amplifier as set forth in claim 46, further comprising:

a transistor differential pair with a source which is connected to respective outputs of the unit circuits; and

a load impedance which connects outputs of the transistor differential pair to a power source,

wherein gates of transistors which make up the transistor differential pair receive oscillation signals which are 180° out of phase from each other.

52. (withdrawn) The variable gain amplifier as set forth in claim 46, comprising:

a variable impedance current mirror circuit, in replacement of the current path control section, which is made up of a plurality of unit current mirror circuits which are disposed parallel to one another and connected to one another through current inputs and current outputs of the unit current mirror circuits, each of the unit current mirror circuits including a first transistor, a second transistor which is paired with the first transistor to make up a current mirror, and a switch circuit which switches levels of operation control voltages for the first and second transistors.

53. (withdrawn) The variable gain amplifier as set forth in claim 47, further comprising:

a current source which supplies a constant current to the current control transistor of each unit circuit.

54. (withdrawn) The variable gain amplifier as set forth in claim 47, wherein:

the switch control signal takes a value of either 0 or 1 to activate or deactivate the current control transistor, and

a channel width of the amplifying transistor satisfies

$wi = W0 \times R^{i} - W0 \times R^{(i-1)}$,

where R is a constant which satisfies

$R = (Wk/W0)^{1/k}$,

where wi is a channel width of the amplifying transistor of the unit circuit which corresponds to the switch control signal of an ordinal number i (0, 1, 2, ..., k; where k is an integer of not less than 0), and Wi is a channel width of i numbers of amplifying transistors whose gain is obtained when i is increased step-wise from 0 by the increment of 1 to increase the number of activated unit circuits according to the operation control voltage which was selected according to the switch control signal to activate the unit circuits.